A-D Subcommittee

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- **Members:** Al Franck, Casey Seino, Mike Shea
- Goals
  - Understand the user requirements
  - Consider:
    - various designs
    - packaging options
    - Costs
  - Propose a design
- Report back to the full group

User Requirements

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- "Survey" a few users
  - Gerry Jackson
  - Bill Marsh
  - Bob Webber
  - Milorad Popovic
  - Chuck Schmidt, Larry Allen
  - Elliott McCrory
- Digitize rate, resolution, packaging

Slow Data, Fast Data Model

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- Two major categories of digitized data
  - “Slow” data (up to few kHz)
    - Continuous data
    - Parameter page readings
    - Fast Time Plot data
    - Snapshot plots up to several kHz digitize rate
  - “Fast” Data
    - Snapshot plots up to 10-20 MHz digitize rate
    - Once only, or repetitive (15 Hz)

Packaging

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- VME-based Digitizers
  - Easy register access by host computer
  - Need to shut down VMEbus Crate to service
  - Difficult cabling
    - Cables in the front or
    - Additional connectors, transition module in the rear
- Remote A-D chassis with serial connection
  - Accessible for service w/o powering down the VMEbus host
  - More flexible cabling
  - Serial Interface to Host mezzanine card (PMC or IP)
  - Memory-like access to control registers

Specific Proposal

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- Remote chassis
  - Fast LVDS serial connection, TX-RX
  - PMC or IndustryPak Interface at host
  - Slow Data
    - 64 ch, differential input,16 bit resolution,14 bit accuracy
    - 4 digitizers, 250 kHz, multiplexed 16 ch each
    - Covers the range DC - 10 kHz
    - Circular buffer at host, 1 sec long
  - Fast Data
    - 8 channels, 12 bit digitizer
    - Digitizer per channel
    - FIFO per digitizer
    - Covers the range 10-20 kHz up to 10 MHz
    - 16k samples per channel

Slow Digitizer: Software Considerations

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- NO software in remote chassis - FPGA Control
- Initialization at Reset time
- Data retrieved by hardware
- Memory Mapped circular buffer
  - 10 kHz data for each of 64 channels
  - Buffer length is 1 sec
- Data is time-stamped by host
  - Interrupt after 64-ch scan (after 10 scans?)
  - Memory pointer register is readable

Fast Digitizer: Software Considerations

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

- NO software in remote chassis- FPGA Control
- Initialization registers
  - Triggering specification
  - Digitize rate
- Triggering parameters
  - Single Snapshot, Repetitive
  - TClk Event + delay, Ext trig, Ext rate
- Memory mapped data
  - Data retrieved by hardware
  - Interrupt when data is available

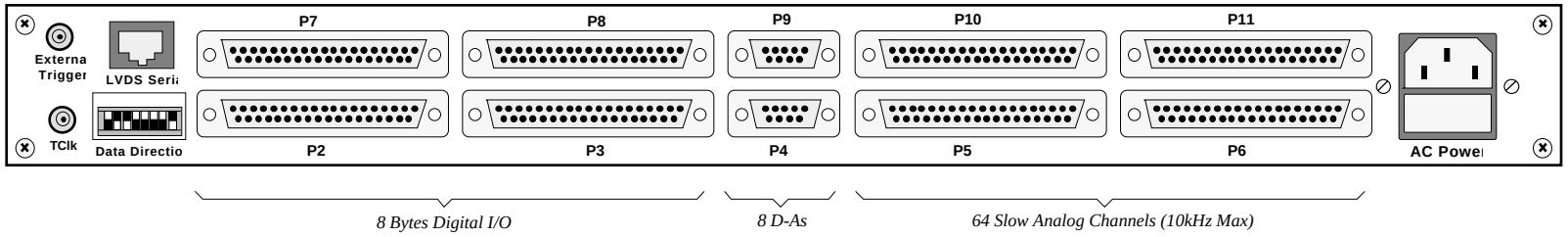
Optional features

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

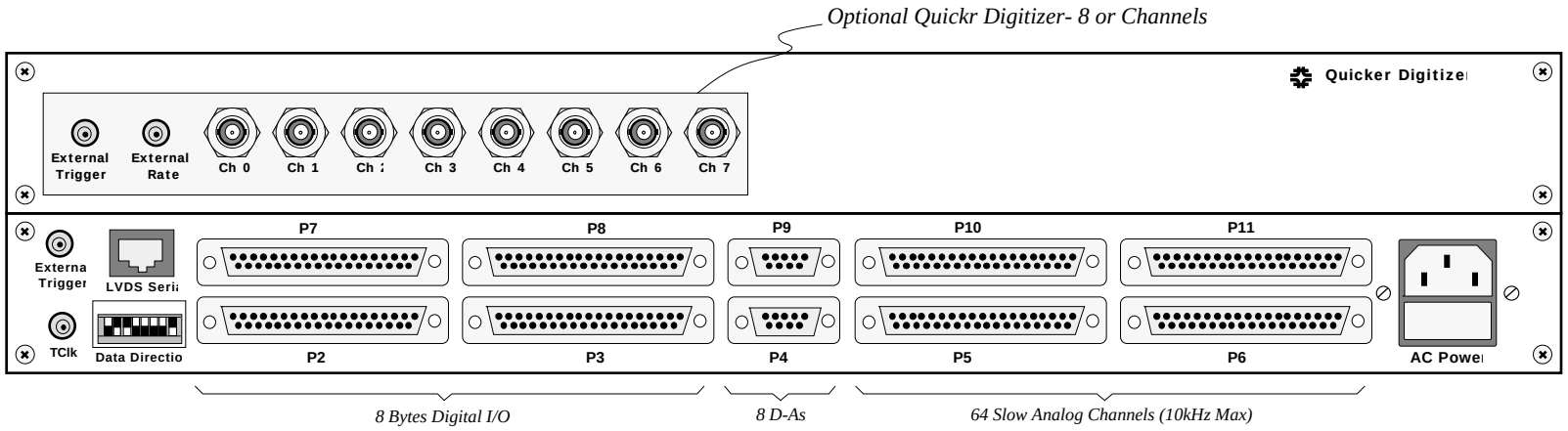
- Include D-A analog outputs
  - 8 Channels, 16 bit resolution, +/- 10 V
  - Used for analog control
- Include Digital I/O (8-bytes)
  - Digital control and readback
  - Stepping motor control
  - OPTO22 connection
  - …..

Physical Implementation

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000



Serial Slow A-D Back Panel



Serial Slow A-D Back Panel with Optional Quikr Digitizers

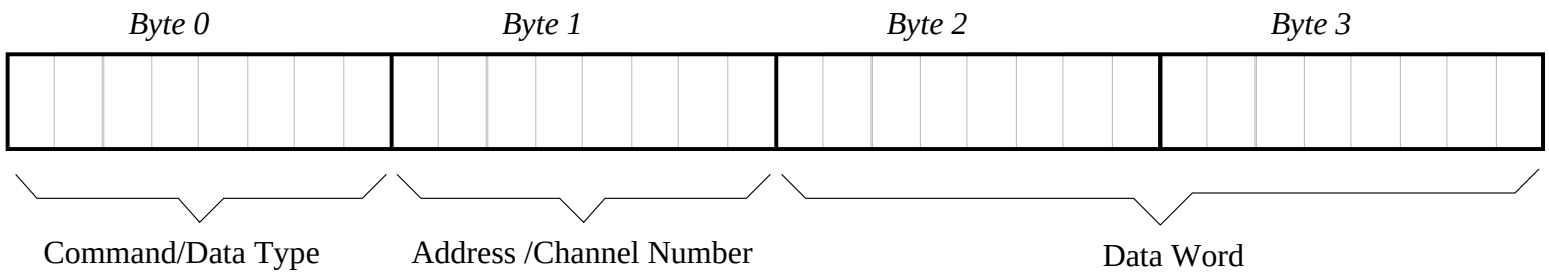
Costs: Remote Unit

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

Enclosure	140
Circuit board	120
Multiplexers	75
Digitizers (4)	140
D-A Converters (2)	60
Altera EPLD	75
LVDS Serial Link	35
Logic, Passive parts	60
Connectors	100
Assembly	100
Power Supply	75
Total	$975
Quikr Digitizer ($100/channel)	$800

Serial Data Format

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000



Format of Serial Transmission Double Word

Costs: Host Interface (PMC)

Al Franck,
Casey Seino,
Mike Shea
March 21, 2000

Circuit board	75
Altera EPLD	100
LVDS Serial Link	35
FIFOs	25
Connectors	25
Misc Logic, Passive parts	50
Assembly	50
Total	$360